Analog very large-scale integrated (VLSI) implementation of a model of amplitude-modulation sensitivity in the auditory brainstem

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(Received 4 February 1998; revised 31 August 1998; accepted 29 October 1998)

An analog very large-scale integrated (VLSI) implementation of a model of signal processing in the auditory brainstem is presented and evaluated. The implementation is based on a model of amplitude-modulation sensitivity in the central nucleus of the inferior colliculus (CNIC) previously described by Hewitt and Meddis [J. Acoust. Soc. Am. **95**, 2145–2159 (1994)]. A single chip is used to implement the three processing stages of the model; the inner-hair cell (IHC), cochlear nucleus sustained-chopper, and CNIC coincidence-detection stages. The chip incorporates two new circuits: an IHC circuit and a neuron circuit. The input to the chip is taken from a ''silicon cochlea'' consisting of a cascade of filters that simulate basilar membrane mechanical frequency selectivity. The chip which contains 142 neurons was evaluated using amplitude-modulated pure tones. Individual cells in the CNIC stage demonstrate bandpass rate-modulation responses using these stimuli. The frequency of modulation is represented spatially in an array of these cells as the location of the cell generating the highest rate of action potentials. The chip processes acoustic signals in real time and demonstrates the feasibility of using analog VLSI to build and test auditory models that use large numbers of component neurons. [S0001-4966(99)03102-1]

PACS numbers: 43.64.Qh, 43.64.Bt [RDF]

INTRODUCTION

The complexity of auditory signal processing in the auditory periphery and brainstem requires sophisticated modeling techniques. Computational modeling of individual stages has already been shown to be a successful approach to characterizing the processes involved. However, when it is necessary to characterize the response of the system as a whole, even high-speed computers may require very long run times. There are approximately 10 000 inner-hair cells (IHCs), 30 000 afferent auditory-nerve (AN) fibers and tens of thousands of neurons in the cochlear nucleus alone. Very large-scale integrated (VLSI) circuitry offers the possibility of evaluating such complex models in real time. Below, we present an initial attempt to exploit analog VLSI technology to simulate a complex system involving inner-hair cells, ventral cochlear nucleus (VCN) sustained-chopping stellate cells, and coincidence-detecting neurons in the central nucleus of the inferior colliculus (CNIC). Although none of the individual cells is modeled in great detail by the electronic circuits, the VLSI system is nevertheless capable of implementing the signal-processing principles exploited by the biological system.

The highly parallel architecture of the auditory periphery and auditory brainstem is well suited to analog VLSI technology because of the case of replicating individual circuits once the design details of a single unit have been decided. For example, all IHCs appear to operate according to the same principles; it is only the input that differs between cells. If a suitable circuit can be designed to simulate their operation, they can be readily replicated in large numbers. The IHC and neurons to be described below occupy approximately the same area on the chip with a density of approximately 4000 neurons (or IHCs) per square centimeter. When IHCs and neurons are combined on a single chip, the response of large assemblies of neurons to complex stimuli is more easily evaluated in real time.

A number of seminal studies using analog VLSI technology have already attempted to simulate individual stages of mammalian auditory-signal processing. Lyon and Mead (1988) produced an early simulation of cochlear mechanical filtering, this has been followed by a number of other studies (Fragnière *et al.*, 1997; Lazzaro and Mead, 1989a; Lyon, 1991; Liu *et al.*, 1991; Sarpeshkar *et al.*, 1996; Watts *et al.*, 1992; Watts, 1993). Lazzaro (1992) has attempted to simulate mechanical-to-electrical transduction analogous to that occurring at the level of the IHC. Others (for example, Mahowald and Douglas, 1991; Mead, 1989; Rasche *et al.*, 1997; Sarpeshkar *et al.*, 1992) have developed models of neurons but only Lazzaro (Lazzaro and Mead, 1989b, 1989c; Lazzaro, 1991) appears to have used VLSI neurons to simulate aspects of auditory processing. In the study described below,

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we build upon these pioneering efforts to show how three different stages of auditory processing can be combined on a single chip to simulate the response of arrays of CNIC units to acoustic stimulation.

The circuit is based on a previous computer model of amplitude-modulation sensitivity of single neurons in the inferior colliculus (Hewitt and Meddis, 1994). The original model was able to simulate the rate response of a single CNIC unit as a function of the rate of amplitude modulation of sinusoidal signals. As such, it represented a testable model of the anatomical and physiological basis of the behavior of these cells as observed in animal preparations (Rees and Palmer, 1989; Langner and Schreiner, 1988). If, however, the model could be extended to represent the simultaneous activity of arrays of such cells, each with a different best-modulation frequency (BMF), its behavior might have relevance to psychoacoustic theories concerning the perception of pitch. Langner *et al.* (1998) have presented evidence that an orderly orthogonal arrangement of cells in the CNIC can be observed with respect to their best frequency (BF) for pure tones and their BMF for modulated tones. While such arrays of cells could be simulated using conventional digital computers, the required processing time can be prohibitive. This was seen as a suitable opportunity to explore the power of analog VLSI circuitry.

Section I summarizes the model as given by Hewitt and Meddis (1994). Section II contains the details of the hardware implementation of the model components. Section III evaluates the model in terms of its ability to represent the behavior of a single CNIC unit. Section IV shows how amplitude modulation may be represented across an array of hardware CNIC cells.

I. MODEL

As far as possible, the hardware was designed to simulate exactly the processing in the four-stage model described by Hewitt and Meddis (1994). This is represented in Fig. 1. Some compromises were necessary when designing the VLSI chip. These will be detailed when describing the hardware implementation in Sec. II. The description immediately below refers to the original software model that inspired the project.

Stage 1 is the mechanical filtering of the cochlea.

Stage 2 is a model of the functioning of an inner-hair cell in response to the mechanical stimulation of the basilar membrane. The model is based directly on that published earlier by Meddis (1986, 1988). The output of the cell is characterized as the probability of occurrence of an action potential in an auditory-nerve fiber synapsing with the cell. An important characteristic of the hair-cell model is that the response adapts over time to a constant stimulus. The output from the cell is half-wave rectified and has a low-pass frequency characteristic with a corner frequency in the region of 1 kHz.

Stage 3 simulates the activity of stellate cells in the VCN that show a sustained-chopping response to pure tones and are thought to have excitatory projections to the CNIC. Each cell receives inputs from a large number of hair cells with similar receptive fields. In the original version of the

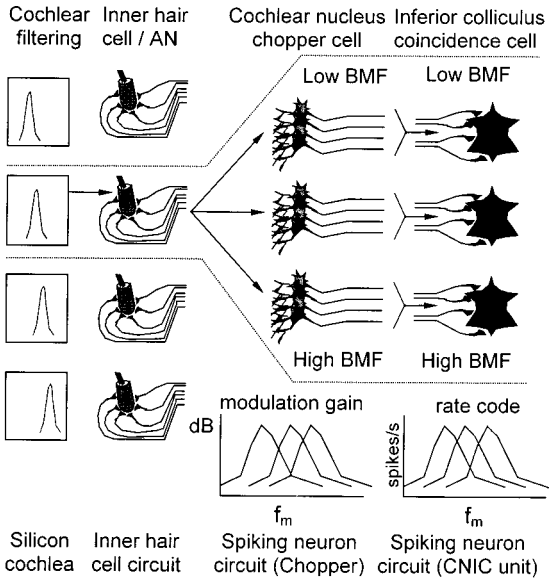

FIG. 1. Proposed neural circuit for amplitude-modulation sensitivity in the inferior colliculus. Abbreviations: BMF-best-modulation frequency. Adapted from Hewitt and Meddis (1994).

model, 60 inputs were used, but later studies (Meddis and O'Mard, 1997) have suggested that 30 might be a more appropriate number. The inputs to a VCN cell are in the form of spikes delivered by auditory-nerve (AN) fibers. They are thought to contact the receiving cell on its dendrites, where substantial low-pass filtering occurs. As a consequence, a continuous, high-frequency tone stimulus results in a steady input current that maintains a steady pressure on the membrane potential and causes it to rise regularly above threshold. The cell responds with a stream of action potentials at a rate determined mainly by its own membrane characteristics (Arle and Kim, 1990; Banks and Sachs, 1991; Hewitt *et al.*, 1992). This rate is its ''intrinsic frequency'' and varies from cell to cell. Detailed studies of models of this process show that these processes can be used to explain the tendency of these cells to synchronize their action potentials to the peaks of amplitude-modulated sinusoids when, and only when, the rate of modulation is close to the intrinsic frequency of the cell (Hewitt *et al.*, 1992).

Stage 4 simulates the observation that some cells in the CNIC respond with a firing-rate increase when the rate of amplitude modulation of a stimulus is close to a narrow range of frequencies characteristic of the particular cell. The model makes the assumption that certain cells in the CNIC receive input from a number of sustained-chopping cells in the VCN and respond only when a number of these inputs are simultaneously active. The inputs are assumed to come from VCN cells with similar intrinsic frequencies. Normally, the spike activity in these inputs will be random with respect to one another, and the CNIC cell will notice few coincidences. However, when the acoustic stimulus is amplitude modulated at a rate sympathetic to the VCN sustained-chopping cells, their activity will be synchronized as each cell spikes at the crest of the amplitude-modulation wave. As a result, the CNIC cell will receive many coincidental inputs and will respond with an increased rate of firing. This model has been shown to simulate rate-modulation functions ob-

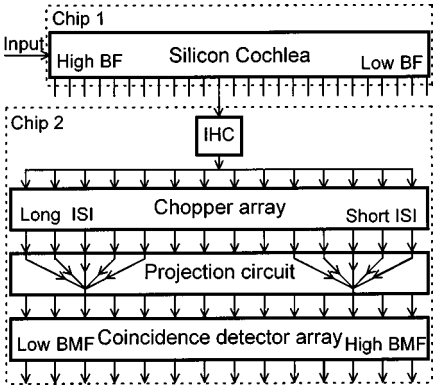

FIG. 2. Implementation of the amplitude-modulation sensitivity model.

served in cells in the inferior colliculus (Rees and Palmer, 1989) It is important to note that the rate–BMF of the CNIC cell depends upon the intrinsic frequencies of the VCN cells that are providing its input. It depends only weakly upon the membrane characteristics of the CNIC cell itself.

II. HARDWARE IMPLEMENTATION

The software implementation is based on carefully modeled individual cells. This would be very hard to achieve with the hardware implementation, since hardware implementations do not have the flexibility or the precision of software implementations. A detailed hardware model of an individual neuron can only be implemented with large and complex circuits (see, for instance, Rasche *et al.*, 1997), which would prohibit the implementation of a large number of these neurons on a single chip. The main advantage of a hardware implementation, however, is that it can simulate a model in real time, even when the number of elements and stages in the model becomes large. We have therefore kept the individual elements small and simple, under the hypothesis that the signal processing in the brain that we try to model depends more on the availability of a large number of neurons than on the exact details of operation of each individual neuron.

The hardware model (Fig. 2) aims to implement the signal processing performed at the different stages of the software model presented in the previous section, not the details of each element. In fact, we only use naming such as IHC, cochlear nucleus (CN) chopper and CNIC to allow the reader to compare the stages in the hardware with those in the original model. They do not imply that the hardware elements are detailed models of their biological counterparts.

The VLSI implementation uses two chips (Fig. 2). The first chip is an electronic simulation of the mechanical filtering of the cochlea and consists of series of bandpass filters corresponding to stage 1 in the model description above. This silicon cochlea has already been described in detail by van Schaik *et al.* (1995). This chip has a number of outputs, each simulating the response of the basilar membrane at a different point along its length. Only one output is fed to the second chip. As a consequence, each chip represents a single frequency-selective ''channel'' and additional chips will be required to represent the full range of channels. For all of the evaluations described below, the center frequency (CF) of the cochlear filter is set to 5 kHz.

The second chip contains the hardware implementation of stages 2–4 of the model: one inner-hair cell (IHC) circuit that models the average output of several IHCs from a small section along the basilar membrane and two arrays of the same spiking neuron circuit, simulating the signal processing of neurons in the VCN and the CNIC, respectively. The same spiking neuron circuit is used to simulate a sustained chopper (VCN) or a coincidence detector neuron (CNIC). Technical details concerning component values are given in the Appendix (see also van Schaik, 1997).

A. Inner-hair cell circuit

The IHC stage is implemented using three main circuit components (Fig. 3). The first component simulates the asymmetrical, saturating response of the IHC receptor potential to mechanical deflection of the stereocilia. It consists of two stages: a compressive function and a circuit to add a bias to the membrane potential. The bias also guarantees spontaneous activity in the absence of any input. The second component implements the low-pass filtering of the membrane potential. The third component introduces adaptation to constant stimulation. The output of the circuit is a continuous current, which can be interpreted as the instantaneous spike probability on a biological auditory nerve. Alternatively, we can interpret this output as the equivalent of the excitatory postsynaptic current generated in a chopper cell by a number of AN fibers from a small section along the basilar membrane that contact this chopper cell. The hardware implementation does not attempt to replicate the detailed mechanisms of the IHC model used in the original paper, but does simu-

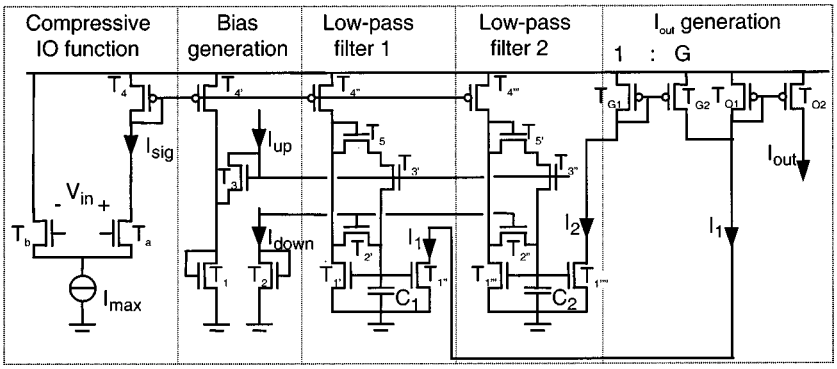

FIG. 3. Circuit diagram for the IHC stage.

late those features of the IHC response to acoustic stimulation that are important for the operation of the AM sensitivity model.

1. Static inner-hair cell voltage response

Hudspeth and Corey (1977) have shown that the relation between bundle deflection and the percentage of open-ion channels has a sigmoidal form with a certain offset, so that 20% of the channels are open at equilibrium. This can be easily modeled using two transistors T_a and T_b) as a differential pair (see Fig. 3) for which the current I_{sig} through transistor T_a is a sigmoidal function between 0 and $I_{\max}$ of the input voltage V_{in}, as we shall see in the measurement of Fig. 4(a). By using a differential pair with one transistor (T_b) four times as large as the other (T_a), only 20% of the bias current will flow through the smaller transistor (T_a) when V_{in} equals zero.

2. Dynamic IHC voltage response

The phase locking of the inner-hair cell can be modeled using a low-pass filter with a cutoff frequency of about 1 kHz (Rose *et al.*, 1967; Palmer and Russell, 1986). This implies a time constant equal to $\tau = 1/2\pi f = 0.16$ ms to model this effect. Obtaining such large time constants is one of the main problems in modeling comparatively slow brain elements with analog VLSI circuits. If the precision of the value of the time constant is not an important issue, then large time constants can be realized using the current mirror shown in the low-pass filter blocks in Fig. 3. This current mirror creates a nonlinear low-pass filter for which I_{up} controls the maximum rise speed and I_{down} sets the maximum fall speed of the voltage on the capacitor C_1. Using this circuit, the time constant will vary as a function of signal level for both the low-pass filter and the adaptation circuits. The time constant can be increased by as much as a factor of 3 for a 20-dB increase in signal level. This is a problem, and to avoid any difficulties in evaluating the later stages, all tests were made at the same signal levels.

3. IHC adaptation

A form of adaptation similar to the adaptation seen on the auditory nerve can be obtained in the IHC circuit by taking a weighted difference between I_1 and a second low-pass-filtered version of I_{sig}. When we use a larger capacitor in the second filter, its output I_2 will react more slowly to an onset of I_{sig} than I_1 does. In the circuit, the value $C_2 = 3C_1$ is used. The actual output current of the IHC circuit is given by $I_{\text{out}} = I_1 - GI_2 + I_{\text{spont}}$ and is created with two additional current mirrors, as shown in Fig. 3. The value G is the gain of this additional current mirror and controls the ratio between the peak response and the sustained response of the circuit. G should be smaller than 1 in order to keep a sustained response to the input signal. I_{spont} can be used to adapt the ''spontaneous rate of firing'' of the inner-hair-cell model independently of the signal levels of I_1 and I_2.

4. Test results

Figure 4(a) shows the measurements of the current I_1, which is the equivalent of the receptor potential in the real inner-hair cell, as a function of the input voltage. Comparison with the intracellular-voltage response to hair displacement as measured by Hudspeth and Corey (1977) shows good agreement. Although the differential pair has been designed to have an output current equal to 20% of the maximum current at zero input voltage, the measurement shows an output current equal to 30% of the maximum current in this case. This is probably due to the mismatch of the differential pair transistors.

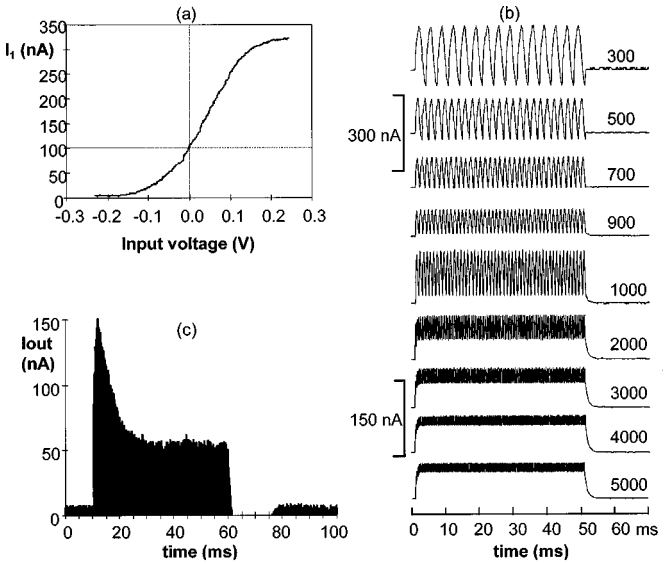

FIG. 4. IHC circuit output. (a) Static relation between I_1 and V_{in}, (b) variation of I_1 for pure-tone inputs at different frequencies, (c) Output current of the IHC circuit after weighted subtraction of I_2 from I_1.

Figure 4(b) shows the response of the current I_1 to pure-tone stimulation at frequencies between 300 Hz and 5 kHz. These results are comparable to those of Palmer and Russell (1986).

The final output current of the circuit in is given by $I_{\text{out}} = I_1 - GI_2 + I_{\text{spont}}$. Using I_{spont}, G, V_{up}, and V_{down} creates an output signal [Fig. 4(c)] similar to the post stimulus time histogram (PSTH) of a single auditory nerve when stimulated with a 5-kHz pure tone. The time constant of adaptation is around 10 ms.

5. Other IHC circuits

The only other analog VLSI implementation of an inner-hair cell known to the authors was implemented by Lazzaro (1992). The circuit is of a size and complexity comparable to the circuit presented here, but does not model the low-pass-filtering behavior of the IHC that causes a reduction in phase locking at frequencies above 1 kHz. This reduction of phase locking is essential for the operation of the AM sensitivity model.

B. Basic neuron circuit

The neuron implementation [Fig. 5(a)] has been kept as simple as possible in order to maximize the number of neurons that could be included on a single chip of size 5 mm^2. The circuit models the main features of a neuron needed to obtain chopping or coincidence-detecting behavior. It con-

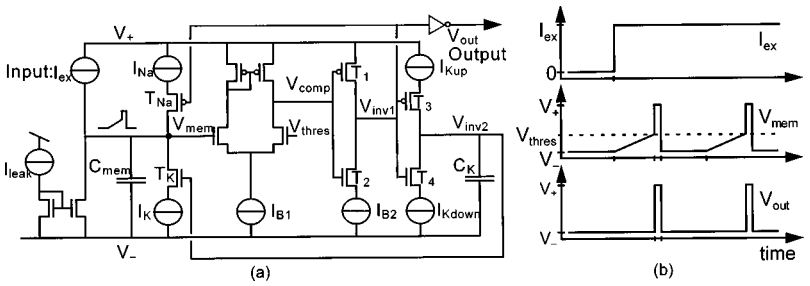

FIG. 5. (a) Circuit details of the VLSI neuron. (b) Example of the response of the membrane potential (V_{mem}) and the output signal (V_{out}) to a dc input current (I_{cx}).

sists of three main components corresponding to auditory-nerve input, membrane potential, and spike generation, respectively.

1. Neuron membrane potential

The membrane of a biological neuron is modeled by a membrane capacitance, C_{mem}; the membrane-leakage current is controlled by the current source, I_{leak}. In the absence of any input ($I_{\mathrm{ex}}=0$), the membrane voltage will be drawn to its resting potential (controlled by V_-) by this leakage current. Excitatory inputs simply add charge to the membrane capacitance. If an excitatory current larger than the leakage current is injected, the membrane potential will increase from its resting potential. This membrane potential, V_{mem}, is compared with a controllable threshold voltage, V_{thres}, using a basic transconductance amplifier driving a high-impedance load. If V_{mem} exceeds V_{thres}, an action potential will be generated [Fig. 5(b)].

2. Neuron-spike generation

The generation of the action potential in the neuron circuit is patterned after the biological neuron, in which an increased sodium conductance creates the upswing of the spike and in which the delayed blocking of the sodium channels plus delayed increase of the potassium conductance creates the downswing. The circuit model is as follows: If V_{mem} rises above V_{thres}, the output voltage of the comparator V_{comp} will rise to the positive power supply. The output of the following inverter V_{inv1} will thus go low, thereby making the *p*-channel metal oxide (PMOS) transistor $\mathrm{T_{Na}}$ conduct and thus allowing the current I_{Na} to pull up the membrane potential. At the same time, however, a second inverter will allow the capacitance C_K to be charged at a rate controlled by the current I_{Kup}. As soon as the voltage V_{inv2} on C_K is high enough to allow conduction of the *n*-channel metal oxide (NMOS) transistor T_K whose gate it controls, the current I_K will be able to discharge the membrane capacitance.

Two different time constants govern the spike-generation process. The current I_{Kup} which charges C_K controls the spike width, since the delay between the onset of conduction of $\mathrm{T_{Na}}$ and the onset of conduction of T_K is inversely proportional to I_{Kup}. If V_{mem} now drops below V_{thres} the output of the first inverter V_{inv1} will become high, blocking conduction of $\mathrm{T_{Na}}$ cutting off the current I_{Na}.

Furthermore, the second inverter will then allow C_K to be discharged by the current I_{Kdown}. If I_{Kdown} is small, the voltage on C_K will decrease only slowly, and as long as this voltage stays high enough to keep T_K conductive and allow I_K to discharge the membrane, it will be impossible to stimulate the neuron if I_{ex} is smaller than I_K. Therefore I_{Kdown} can be said to control the ''refractory period'' of the neuron.

Finally, I_{B1} and I_{B2} are two bias currents needed to limit the power consumption of the circuit; they do not influence the spiking behavior of the neuron in any major way.

3. Other neuron circuits

Several analog VLSI neurons have been published (for example, Mahowald and Douglas, 1991; Lazzaro and Mead, 1989a; Mead, 1989; Rasche *et al.*, 1997; Sarpeshkar *et al.*, 1992), and they can be divided into two categories. The first category, which contains the neuron circuit presented here, was started by Mead (1989). It uses a small circuit as a neuron model that tries to capture just the essentials needed for a given processing task. The goal in this case it to put a large number of these neurons on a chip to study their behavior as a group. Most of the neurons published in this group, however, are too simple for the AM sensitivity model, because they do not implement a refractory period, which is needed to control the intrinsic chopping rate of the choppers, nor do they include membrane leakage, which is needed to set the temporal selectivity of the coincidence-detector neuron. One neuron circuit, published by Sarpeshkar *et al.* (1992), is very similar to the neuron circuit presented here and could have been used for the AM sensitivity model. The circuit presented here is just slightly larger, but allows parameters such as the spiking threshold, spike width, and refractory-period duration to be controlled independently, which is not the case in Sarpeshkar's neuron. The second category of neuron circuits, started by Mahowald and Douglas (1991), tries to model a single neuron in great detail by implementing the hardware equivalent of Hodgkin–Huxley models. These neuron circuits, however, are not useful for the implementation of the AM sensitivity model because they are simply too big. For example, a recent publication of such a neuron by Rasche *et al.* (1997) describes a chip of the same size as our complete AM sensitivity model (4 mm^2), but the chip contains only a single neuron that emulates a cortical pyramidal cell.

C. VCN sustained-chopper model

The input to the neuron comes directly from the IHC and is a current representing the probability of an action potential in the afferent auditory-nerve fibers that contact a real VCN chopper neuron. Ideally, this should be in the form of discrete, stochastic spike events. Unfortunately, the generation of random events proved difficult using this technol-

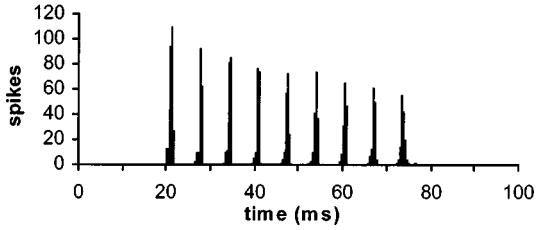

FIG. 6. Measured sustained-chopping response of a neuron on the chip.

ogy. The use of probabilities is not problematic for this particular application because the input to real cells comes from a large number of fibers and is strongly low-pass filtered at the cell dendrite. The net effect is roughly the same, but the electronic neuron remains more regular, i.e., sustains chopping longer, than its biological counterpart. The difficulty in generating random spikes will need to be overcome in the future, however, for other applications such as bushy cells. The neuron circuit described above (in conjunction with the IHC circuit) produces a sustained-chopping response when stimulated with a 5-kHz pure tone (Fig. 6). The rate at which the cell chops is controlled by the current I_{Kdown}, which is varied systematically across the array. The minimum- and maximum-chopping rates used for this project were 90 and 180 spikes per s, respectively.

D. VCN–CNIC projections

Each CNIC unit receives input from a range of VCN neurons at the previous level. The width of this range can be varied under operator control. The strongest input comes from the corresponding neuron in the VCN array. Inputs to the left and right are attenuated by a factor depending upon the distance from the CNIC unit to the VCN unit. The circuit that creates this connectivity, shown in Fig. 7, uses only two transistors, one input wire, and one output wire per CNIC neuron.

The operation of this circuit may be understood as follows: When a spike arrives at synapse 3, for instance, the current I_{syn3} will flow through the switch for the duration of the spike. Part of this current will flow directly through the transistor T_{G3}; the output current I_{ex3} will be equal to this

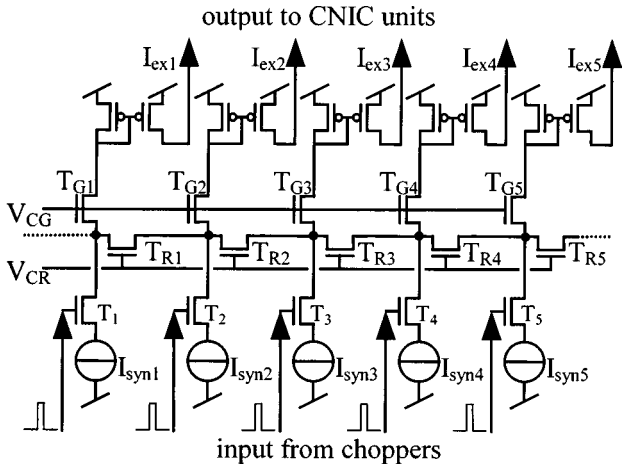

FIG. 7. The lateral-diffusion network circuit.

current. The rest of the current flows into the network to either side of the node which connects the different synapses laterally. If we assume that the network extends infinitely to the left and to the right, equal amounts of current will flow left and right. At the neighboring nodes these currents will split again, partially continuing to flow through the lateral transistors and the rest creating the output currents I_{ex2} and I_{ex1}. In this way, a current injected at a certain node in the network creates a symmetrical distribution of output currents; the largest output current occurs at the same node as the injection, and the amplitudes of the output currents decrease as the node gets farther away. It can be shown that when the transistors are operated in the weak inversion region, the distribution of currents is an exponential function given by:

$$\frac{I_{\mathrm{exj}}}{I_{\mathrm{syni}}} = \alpha e^{-d_{ij}/L}, \quad \alpha = \frac{1-e^{-1/L}}{1+e^{-1/L}}, \quad L = e^{(V_{CG}-V_{CR})/2nU_T}, \tag{1}$$

where d_{ij} is the distance in number of lateral transistors between output j and input i, n is the slope factor of the transistors (about 1.5), and U_T is the thermal voltage, which is 25 mV at room temperature. V_{CG} and V_{CR} are the bias voltages that are used to set L. In the experiments of this paper, a diffusion length L of about 3 has been used. Furthermore, since the circuit is completely linear in the current domain, we can apply the superposition principle, so that the current at a given output node is simply the sum of the individual effects of the input currents at the input nodes.

E. IC coincidence-detecting neuron model

The neuron circuit of Fig. 5 can also be used to create a coincidence-detecting neuron. In this case, the membrane time constant should be short, so that the neuron does not integrate its input over an extended period of time. If the input to the neuron consists of excitatory current spikes with an amplitude that ensures that no single spike can make the membrane potential reach the threshold voltage, multiple spikes will have to arrive simultaneously, or in very quick succession, in order to create output spikes. A way to reduce the membrane time constant is to reduce the membrane capacitance C_{mem}, which also saves considerable silicon area, since the capacitors are the largest structures on the chip. The second capacitor C_K can also be reduced in size to save space since the refractory period of the coincidence-detector cell does not play as important a role as it does for the chopper neuron.

III. SINGLE-UNIT SIMULATION

The output of the three types of units in the VLSI model has been characterized (Fig. 8) as a function of input-signal intensity, using a 5-kHz pure tone filtered by the silicon cochlea and taken at the output of the cochlear filter with a 5-kHz best frequency. The input intensity that just evokes spikes from the CN unit has been chosen as the 0-dB point. The IHC circuit does not actually generate spikes, but its current output is representative of a spike probability; in order to present it in the same graph, the current has been

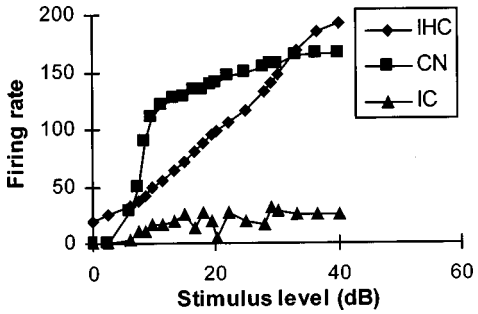

FIG. 8. Rate-intensity functions of the three types of units in the VLSI model for a 5-kHz pure-tone input. Stimulus intensity is given in dB relative to the spiking threshold of the CN unit.

converted into a spike rate, using an arbitrary scaling factor. Saturation of the IHC output, which is shown in Fig. 3(a), cannot be measured in the complete system, because the silicon cochlea cannot deal physically with sounds of such large amplitude. We do see in Fig. 8, however, that both the CN unit and the inferior colliculus (IC) unit saturate before the IHC unit does.

The spike activity of a chopper circuit will synchronize to the envelope of an amplitude-modulated, high-frequency tone. This will only occur, however, when the rate of AM is similar to the intrinsic rate of firing of the cell as controlled by the current I_{Kdown}. While synchronization is best at a particular frequency, it will still occur to a narrow range of frequencies above and below its best-modulation frequency. For any given rate of AM, some choppers will produce a stream of spikes synchronized with the amplitude modulation. As a result, the spikes produced by this group will be synchronized with each other and capable of driving a coincidence detector.

Synchronization of similar choppers by amplitude modulation at the appropriate modulation frequency can be seen in the oscilloscope traces of Fig. 9. When the input signal is either above or below BMF, the choppers do not synchronize to the input signal, and they therefore do not synchronize to each other either.

Activity in a coincidence-detector (CD) cell is generated by synchronized inputs from the chopper neurons. Pure-tone stimuli do not produce correlated activity across neighboring chopping cells, and they do not produce a rate rise in these CD units. Neighboring choppers with similar BMFs are connected to a single CD coincidence detector through the lateral-diffusion network. This network ensures that the CD unit is most strongly stimulated by a single chopper and that the neighbors of this chopper on either side stimulate the CD unit with a strength that falls off with distance. When this network is used with a diffusion length of about 3, then only three choppers on either side of the central chopper will have a noticeable effect on the CD unit. The CD input current will thus be maximal when these seven choppers spike simultaneously. The threshold of the CD unit can be set to require seven simultaneous input spikes using the I_{syni} current source (Fig. 7). When this is the case, the CD unit will only generate a spike if the inputs are perfectly correlated, i.e., when an appropriate modulation frequency is present. However, this setting would allow very little variation in the intrinsic chopping rate of the chopper units on the chip. In order to relax the constraints a little, the threshold has been adapted so that three neighboring chopper units spiking simultaneously are sufficient for reaching the threshold of firing of the CD cell. Furthermore, the oscilloscope trace in Fig. 9 shows very little noise on the IHC output. With such a deterministic IHC output, the synchronization will be far stronger than in biology at the BMF, and also disappear more quickly for frequencies above or below BMF. We have also observed very strong synchronization of the choppers to every second or third cycle of AM for modulation frequencies close to two or three times the BMF of the unit when this stimulus is used. In order to obtain a more biological behavior of both the chopper units and the CD units, we have explicitly added noise to the IHC output current. We have increased the noise level and measured the synchronization of the choppers to the signal [Fig. 10(a)], until the degree of synchrony to the stimulus envelope of the evoked activity of a chopper unit at different modulation frequencies roughly matches that of a biological chopper and of the computer model as presented by Meddis and O'Mard (1997). The sensitivity of the CD unit using these settings to amplitude modulation is shown in Fig. 10(b) for a single unit on the chip. Unfortunately, no data was available for a real IC neuron with a best-modulation frequency in the 130-Hz range. We have therefore plotted the data for a 52-Hz BMF unit from the Hewitt and Meddis' (1994) paper in the same figure (original data from Rees and Palmer, 1989). It can be seen that the VLSI CD unit has a more selective modulation-transfer function (MTF) than the IC neuron, but is of the same order of magnitude and shape.

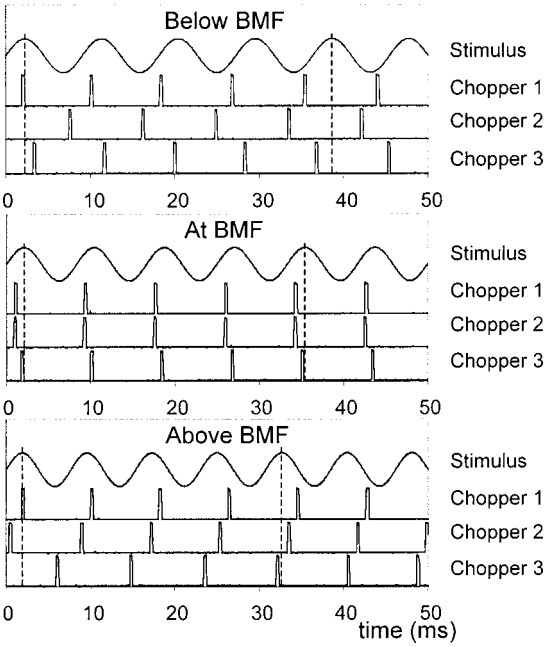

FIG. 9. Oscilloscope traces of the input signal to the IHC circuit and the output traces of three similar choppers on the chip; (a) below BMF, (b) at BMF, and (c) above BMF.

The degree of synchrony for the choppers has been measured from their period histograms using the vector-strength metric (Goldberg and Brown, 1969). Vector strength (r) is calculated as:

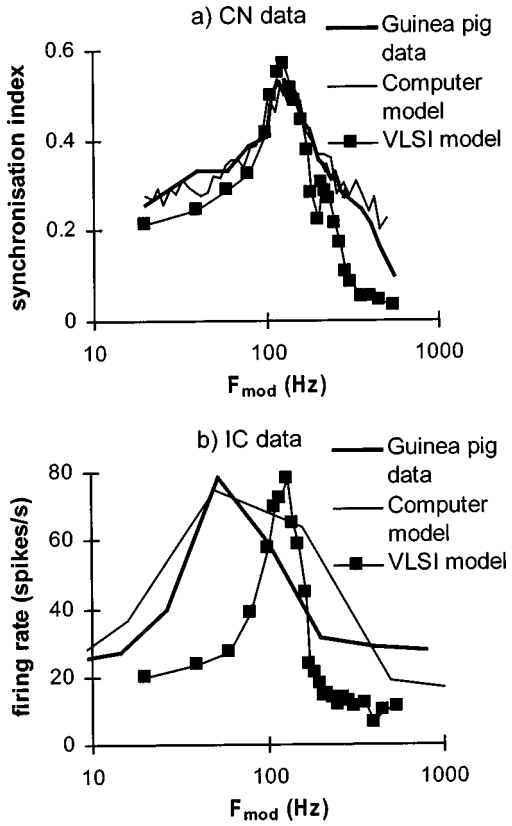

FIG. 10. (a) Vector strengths for the CN unit measured on guinea pig and Meddis' original computer model (Meddis and O'Mard, 1997) and the VLSI implementation. (b) AM sensitivity of an IC coincidence-detecting unit.

$$r = \frac{\sqrt{[\Sigma_0^{K-1} R_k \cos 2\pi(k/K)]^2 + [\Sigma_0^{K-1} R_k \sin 2\pi(k/K)]^2}}{\Sigma_0^{K-1} R_K}, \tag{2}$$

where K is the number of bins in the period histogram, and R_k is the magnitude of the kth bin.

IV. MULTIUNIT REPRESENTATION OF AM SENSITIVITY

While physiological studies are typically restricted to the measurement of the response of a single cell, the modeler can simulate the simultaneous response of large numbers of units. An overview of the operation of the chip as a whole is shown in Fig. 11, which illustrates measurements of the choppers and the coincidence detectors, respectively. In order to show the principle of operation clearly, a non-noisy output of the IHC circuit has been used for these measurements. Figure 11(a) shows the chopping rate of all choppers in the array when stimulated with a 5-kHz pure tone. The chopping rate increases along the array for a given stimulus intensity, due to the decreasing refractory period of the choppers in the array. Because of unavoidable component mismatch, the chopping rate, or intrinsic frequency of the cell, is a noisy function of the position in the array.

Figure 11(b) shows the spiking rate of the choppers when stimulated with a 5-kHz signal which is amplitude modulated at 120 Hz at 50% modulation depth. Most choppers are unaffected by the introduction of modulation, but those units whose intrinsic frequencies are close to 120 Hz

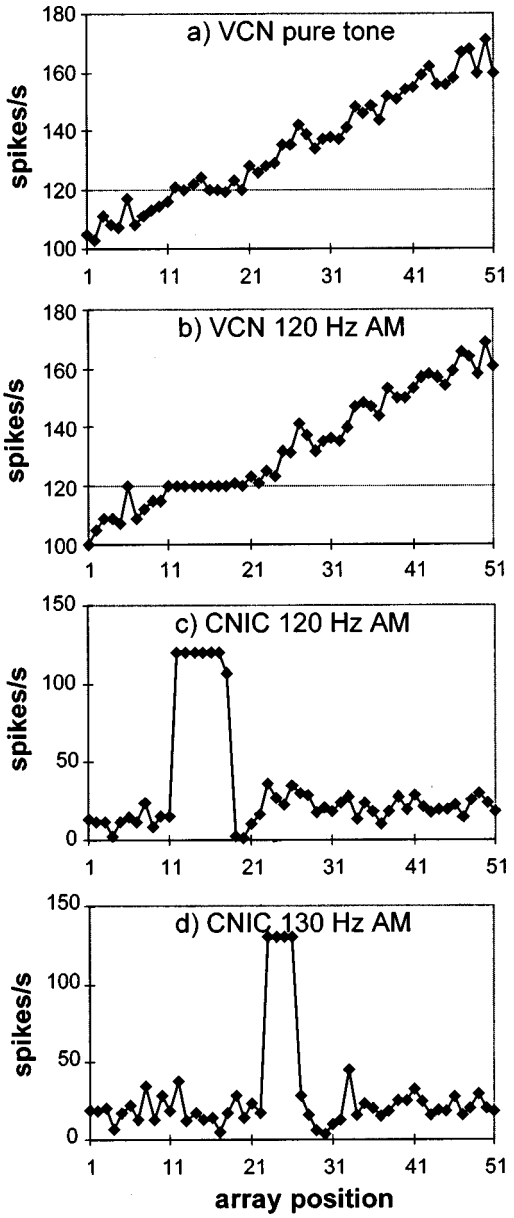

FIG. 11. (a) Average spiking rate of the choppers in the array in response to a pure-tone stimulus. (b) Average chopping rate in response to the pure-tone amplitude modulated at 120 Hz and 50% depth. (c) AM sensitivity of the coincidence-detecting neurons in response to the 120-Hz AM stimulus. (d) Response of the coincidence detectors to a 130-Hz AM stimulus. Note that only the central 51 of the 71 neurons in each array are shown.

are recruited to fire at the same rate as the modulation. It is also the case that these choppers fire at the same phase each modulation period, and are therefore phase locked to the modulation signal. The response of the CD neurons to the input from the choppers is summarized in Fig. 11(c). A small range of CD cells shows a high rate of firing. These are the cells that receive input from the choppers that are synchronized to the 120-Hz amplitude-modulated input signal. Figure 11(d) shows the response for a signal modulated at 130 Hz. The position of the responding CD unit moves to the right of the array. There are fewer CD neurons responding to the 130-Hz modulation than to the 120-Hz modulation, i.e., the peak in Fig. 11(d) is narrower than the peak in Fig. 11(c). This is caused by the random variations of component values

accidentally giving rise to more choppers with an intrinsic chopping rate closer to 120 than to 130 Hz. This fact may be checked in Fig. 11(a).

V. DISCUSSION

The primary goal of this project was to explore the feasibility of using VLSI technology to overcome the speed restrictions inherent in conventional computational modeling of signal processing in the auditory periphery and brainstem. The success of the project suggests that future modeling efforts should definitely consider using this approach. The pressure to use real-time, highly parallel architectures will increase as modelers reach beyond the IC to the thalamus and, eventually, the cortex. VLSI technology appears to have the capacity to meet the additional signal-processing needs. This is especially true for analog VLSI, continuous-time implementations, which operate per definition in real time.

The demonstration has many shortcomings. The project used only a very small chip incorporating one hair cell and 142 neurons. The difficulty experienced in obtaining physiologically accurate cochlear bandpass filters on the input chip restricted the stimuli to pure tones and AM tones that were not affected by this limitation. The IHC circuit has time constants that were dependent (unrealistically) on signal level. We have not been able to solve the problem of how to generate stochastic streams of spikes in the hardware implementation of inputs to the VCN chopper units. The hardware neurons were relatively primitive and only captured the simplest properties necessary to characterize the relevant characteristics of sustained chopping units. These problems will need to be solved before the technology can be used as a general-purpose modeling tool. Nevertheless, the present circuit has demonstrated the feasibility of an alternative approach to modeling complex signal processing in the brainstem.

In fact, the restraints imposed by the new technology did result in some unexpected new perspectives. First, the model works well without a stochastic input to the chopper cells, even though this was assumed to be essential to the success of the original computational model. The low-pass filtering of the dendritic inputs to real VCN choppers is likely, in any case, to attenuate much of the random fine-structure of the AN input. In the hardware model, the natural variation in intrinsic frequency of neighboring choppers is responsible for the decorrelation of spike activity that distinguishes steady-tone stimuli from amplitude-modulated tones. This may also be the case in the auditory nervous system. Second, in the original model, the chopper cells feeding the CNIC coincidence detectors were established as exclusive groups of choppers with identical intrinsic frequencies within a group. This was shown to be unnecessary by the VLSI model, which tolerated limited variation in intrinsic frequency and was able to use the output from one VCN chopper to feed a number of CD cells. This was a useful economy on our small VLSI chip and is a potential economy for the nervous system itself.

In the model, the best rate-modulation frequency of a CD unit is determined by the membrane characteristics of the chopping units that supply its input. The intrinsic chopping rate of the CD cell is not relevant. It is interesting, in this regard, that Rees *et al.* (1997) have recently found that CNIC cells with a highly regular (chopping) response to pure tones are not the cells that have the best response to amplitude modulation. The model described here would predict that a pronounced intrinsic regularity would impair the ability of the CNIC to respond to the intrinsic rhythms of the VCN chopping units, and is therefore consistent with the physiology.

The chip described above contained only 142 neurons. A 1-cm^2 chip could hold 4000 neurons. It is not known how many sustained-chopper cells there are in the VCN, but estimates of the number of multipolar cells (of which only some are sustained choppers) suggest something in the region of 28 000 in the cat (Liberman, 1990). If half of these are sustained choppers and half of the units on the chip are reserved for CNIC units, about eight identical chips would be required to represent a complete model of this AM sensitivity model using 1-cm^2 chips. If, say, 30 chips were used to represent a useful number of channels, each covering a small range of frequencies, there would be space to include other aspects of VCN functioning such as the response of bushy and octopus cells, known to be present in the human cochlear nucleus (Adams, 1996). Each chip would be identical except for the input, which would derive from a different filter tap in the silicon cochlea.

VI. CONCLUSIONS

An analog VLSI device has successfully implemented a model of the complex interaction of a large assembly of neurons in the auditory brainstem thought to be responsible for processing amplitude-modulated acoustic stimuli. The device prepares the way for large-scale implementations representing a similar number of neurons to those found in the mammalian brainstem.

ACKNOWLEDGMENTS

This work was supported by the Swiss National Science Foundation. We are grateful to Eric Fragnière and Eric Vittoz for continuous practical support throughout this project.

APPENDIX

A. Implementation: Technical details

The chip described in this paper has been integrated in ES2's 1.0-μm CMOS technology ECPD 10.

The channel width-over-length ratios (W/L) of the transistors in the IHC circuit and the neuron circuit are given in Table AI and Table AII, respectively. For all measurements a 5-V power supply has been used.

The bias currents of the IHC circuit were determined as follows. $I_{\max}$ directly sets the maximum value of I_1 and has been set to 330 nA, as may be seen in Fig. 4(a). The adaptation gain G was about 2/3, so that the sustained output of the IHC circuit was about 1/3 of the maximum output at the onset of the stimulus, as may be seen in Fig. 4(c). Finally, I_{up}

TABLE AI. IHC circuit-device geometry.

Transistor	W/L (μm)
T_a	5/5
T_b	20/5
T_1, $T_{1'}$, $T_{1''}$, $T_{1'''}$, $T_{1''''}$	5/10
T_2, $T_{2'}$, $T_{2''}$	5/5
T_3, $T_{3'}$, $T_{3''}$	5/5
T_4, $T_{4'}$, $T_{4''}$, $T_{4'''}$	5/10
T_5, $T_{5'}$	2
Capacitor	C (pF)
C_1	5
C_2	15

and I_{down} have been adapted to obtain the output of I_1 for different input frequencies shown in Fig. 4(b) and are both on the order of 0.5 nA.

The design of the neuron has been kept very simple: all transistors that function as switches are 5 by 2 microns and all others are 5 by 5 microns (Table AII). The capacitors C_{mem} and C_K are 10 pF for the chopper implementation and 1 pF for the CD neuron implementation, respectively.

Different bias currents and voltages influence the behavior of the neuron. Some of the variables, however, have little influence, or influence only factors that can be easily fixed, such as the spike width. In order to generate a fixed-width, fixed-height spike, I_{Na} should be much larger than the leakage current I_{leak} or than the input current I_{ex}. In order to be able to bring the membrane potential back down at the end of the spike, I_K should in turn be larger than I_{Na}. The exact values of I_{Na} and I_K, however, are not critical. Both I_K and I_{Na} are currents in the 1-μA range, with I_K about twice as large as I_{Na}. The width of the spike depends almost exclusively on I_{Kup}, which has been adapted to yield a spike 0.3-ms wide. This yields a value for I_{Kup} of about 0.1 μA. The function of the bias currents I_{B1} and I_{B2} is only to limit the current flow through the threshold comparator, and through the first inverter. Their exact value is not important either, and has been set equal to I_K. The threshold voltage V_T influences the time the neuron needs to integrate a constant input from the end of the refractory period to the onset of the output spike. When both the input amplitude and the threshold voltage are doubled, the effective integration time will stay constant. In other words, doubling the threshold voltage is equivalent to reducing the input current by half. In the experiments in this paper, a threshold voltage of 3 V has been used.

The two remaining biases, I_{Kdown} and I_{leak}, have quite a large influence on the spiking behavior of the neuron. I_{Kdown} controls the duration of the refractory period of the neuron, and thereby sets the intrinsic chopping rate or limits the maximum spiking rate of the neuron. I_{Kdown} is made to vary along the chopper array, so that the intrinsic chopping rate of the neurons is 100 spikes per s at one end and 200 spikes per s at the other end. This means that, in either case, the refractory period is at least several ms. In order to create such long refractory periods, I_{Kdown} has to be small, on the order of 1 nA. For the coincidence-detecting neuron, I_{Kdown} is used to limit its maximum rate, which has been adjusted to about 200 spikes per s. The same I_{Kdown} as for the fastest chopper can thus be used for all coincidence-detector neurons.

TABLE AII. Neuron circuit-device geometry.

Transistor	W/L (μm)
T_{Na}, T_K, T_1, T_2, T_3, T_4	5/2
others	5/5
Capacitor	C (pF)
C_{mem}	10, 1
C_K	10, 1

I_{leak} plays an important role in creating the coincidence-detector behavior. The input to the coincidence-detector neuron is in the form of fixed-width, fixed-height current spikes which are passed through the lateral-diffusion network. The amplitude of the output-current spikes of the chopper and the lateral-diffusion length L are set, using I_{syni} and V_{CR} plus V_{CG}, respectively (Fig. 7), so that the input-spike current for the coincidence detector is larger than I_{leak} when the input comes from one of the seven most proximal chopper neurons only. I_{leak}, thus, limits the number of choppers that influence the coincidence detectors for a given setting of I_{syni}, V_{CR}, and V_{CG}. I_{leak} should, however, be used to set the temporal window of the coincidence detection, since it does this independently of other bias values. A relatively high I_{leak} ensures that the membrane potential returns quickly to the resting potential after a single-input spike. When a single-input spike is not strong enough to charge the membrane capacitance up to the threshold voltage, several spikes have to arrive in quick succession to elicit spikes from the coincidence-detector cell. The temporal window within which the spikes have to arrive is controlled by I_{leak}. An I_{leak} on the order of 10 nA has been used, which results in a temporal window on the order of 1 ms. Next, I_{syni}, V_{CR}, and V_{CG} should be adapted to get the desired number of choppers that influence the coincidence detector. Finally, the threshold voltage V_T of the coincidence detector should then be adapted, so that the coincidence detector spikes when a few of the input spikes from the choppers are simultaneous. In order to obtain a diffusion length L on the order of 3, V_{CR} and V_{CG} have been set to 2.66 and 2.74 V, respectively. I_{syni} is about 80 nA and V_T is 3 V.

A difference in the role of I_{leak} for the chopper neurons stems from the fact that the input to the chopper neurons is a directly injected, continuous analog current and not in the form of current spikes. When the membrane potential is at rest, only an input current larger than I_{leak} will be able to drive the membrane potential towards the threshold voltage. When the input current is larger than I_{leak}, the current that effectively charges the membrane capacitor is given by $I_C = I_{\text{ex}} - I_{\text{leak}}$. For the chopper neurons, I_{leak} thus functions as a stimulation threshold and acts to subtract a constant value from the input current. In the tests in this paper, however, I_{leak} has been minimized to a value well below 1 nA and its effect on the chopper neurons is therefore negligible.

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